--The objective of the present invention is to provide a manufacturing method for a semiconductor device which can carry out a polishing process and a dicing process safely without damaging the semiconductor wafer, without causing cracks, and without chipping.--

Please replace the paragraph beginning on page 11, line 22 with the following rewritten paragraph:

--Therefore, it is possible to eliminate the breaking process after the semi-full dicing process that has been conventionally required, to reduce the number of processes, and also to prevent cracks and chips that used to occur at the time of breaking. Thus, it becomes possible to carry out a polishing process and a dicing process safely without damaging the semiconductor wafer, without causing cracks and chips.--

Please replace the paragraph beginning on page 25, line 18 with the following rewritten paragraph:

--The manufacturing method of a semiconductor device in accordance with the present embodiment is a method in which, after a semi-full dicing process has been carried out from the front face (element formation face) bearing semiconductor elements of a disk-shaped semiconductor wafer, processes such as a rear-face polishing process, a dividing process to each piece of chips and a removing process of a damaged layer (defective areas) such as, a machining-affected layer and fine cracks, caused by the semi-full dicing process, are simultaneously carried out.--

Please replace the paragraph beginning on page 30, line 8 with the following rewritten paragraph:

--In the chemical etching process (S6, Fig. 2(f)), with the front face of the semiconductor wafer 1 (element formation face) being protected by the film 13, a damaged area on a cut face 7a of a semiconductor chip 7 resulting from a semi-full dicing process (S3, Fig. 2(c)) is removed by the chemical etching process, and the rear-face polishing process of the semiconductor wafer 1 and the dividing process thereof into individual semiconductor chips 7 are also carried out.--

Please replace the paragraph beginning on page 30, line 17 with the following rewritten paragraph:

-- In other words, the semiconductor wafer 1, affixed onto the film 13 secured to the carrier frame 14, is immersed into, for example, a hydro-fluoric acid based etchant at a normal temperature of 25°C. Thus, while the front face (element formation face) is being protected by the film 13, the semiconductor wafer 1 is chemically etched so that it becomes possible to simultaneously carry out the rear-face polishing process of the semiconductor wafer 1, the dividing process into individual semiconductor chips 7 and the removing process of a damaged layer, such as a machining-affected layer and cracks, in the cut face 7a of the semiconductor chip 7 due to the semi-full dicing process.--

Please replace the paragraph beginning on page 31, line 6 with the following rewritten paragraph:

--In the etchant, first, the semiconductor wafer 1 is etched from the rear face of the semiconductor chip 7 in the thickness direction. In this case, the dicing residual portion is simultaneously etched from the rear face so that when the etching has reached the dicing residual amount of the semi-full dicing process, the semiconductor wafer 1 is separated into semiconductor chips 7. Then, after the separation into the semiconductor chips 7, the etchant enters a groove between the adjacent semiconductor chips 7, with the result that the conductor chip 7 is also etched in the width direction from the cut surface 7a; thus, the damaged layer (defective areas) resulting from the semi-full dicing process is also removed. Here, the application of a bonding agent having a chemical etching resistant property in joining the semiconductor wafer 1 to the film 13 makes it possible to prevent the etchant from entering the bonding face of the semiconductor wafer 1 and from etching the front face (element formation face).--

Please replace the paragraph beginning on page 35, line 23 with the following rewritten paragraph:

-- As described above, even in the case of the application of the device shown in Fig. 5 or Fig. 6, by using the chemical etching process, a damaged layer (defective areas) on the rear face of the semiconductor wafer 3 caused by the polishing process and a damaged layer (defective areas) such as a machining-affected layer and fine cracks in the chip cut face caused by the semi-full dicing process, can be removed while the front face (element formation face) of the semiconductor wafer 3 is being protected, and simultaneously with these processes, the rear-face polishing process of the semiconductor wafer 3 and the separation to individual chips from the

semi-full dicing state through the removal of the dicing residual portion can be carried out at the same time.--

Please replace the paragraph beginning on page 37, line 20 with the following rewritten paragraph:

--Moreover, by adopting a carrier system using a carrier frame 14(14'), the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer 1 or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production.--

Please replace the paragraph beginning on page 38, line 14 with the following rewritten paragraph:

--Referring to Figs. 7 and 8, the following description will discuss another embodiment of the present invention. Here, for convenient explanation, in the present embodiment, those members that have the same functions and that are described in Embodiment 1 are indicated by the same reference numerals and the description thereof is omitted.--

Please replace the paragraph beginning on page 42, line 10 with the following rewritten paragraph:

--In the chemical etching process (S14, Fig. 8(d)), with the front face of the semiconductor wafer 1 (element formation face) being protected by the film 16, a damaged area on a cut face 7a of a semiconductor chip 7 resulting from a semi-full dicing process (S13, Fig.

8(c)) is removed by the chemical etching process, and the rear-face polishing process of the semiconductor wafer 1 and the dividing process thereof into individual semiconductor chips 7 are also carried out.--

Please replace the paragraph beginning on page 42, line 19 with the following rewritten paragraph:

--In other words, the semiconductor wafer 1, affixed onto the film 16 secured to the carrier frame 14', is immersed into, for example, a hydro-fluoric acid based etchant at a normal temperature of 25° C. Thus, while the front face is being protected by the film 16, the semiconductor wafer 1 is chemically etched so that it becomes possible to simultaneously carry out the rear-face polishing process of the semiconductor wafer 1, the dividing process into individual semiconductor chips 7 and the removing process of a damaged layer, such as a machining-affected layer and cracks, in the cut face 7a of the semiconductor chip 7 due to the semi-full dicing process.--

Please replace the paragraph beginning on page 43, line 7 with the following rewritten paragraph:

--In the etchant, first, the semiconductor wafer 1 is etched from the rear face thereof in the thickness direction of the semiconductor chip 7. Simultaneously, since the etchant enters a groove between the adjacent semiconductor chips 7, the dicing residual portion is etched from the rear face so that when the etching has reached the front face (element formation face) of the semiconductor wafer 1 through the dicing residual amount, the semiconductor wafer 1 is

separated into semiconductor chips 7. Moreover, at the same time, the semiconductor chip 7 is also etched in the width direction from the cut surface 7a; thus, the damaged layer (defective areas) resulting from the semi-full dicing process is also removed. Here, the application of a bonding agent having a chemical etching resistant property in affixing the semiconductor wafer 1 onto the film 16 makes it possible to prevent the etchant from entering the bonding face of the semiconductor wafer 1 and from etching the front face.--

Please replace the paragraph beginning on page 44, line 22 with the following rewritten paragraph:

--Moreover, by adopting a carrier system using the carrier frame 14', the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer 1 or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production.--

Please replace the paragraph beginning on page 46, line 23 with the following rewritten paragraph:

--Referring to Figs. 9 and 10, the following description will discuss still another embodiment of the present invention. Here, for convenient explanation, in the present embodiment, those members that have the same functions and that are described in Embodiments 1 and 2 are indicated by the same reference numerals and the description thereof is omitted.--

Please replace the paragraph beginning on page 50, line 8 with the following rewritten paragraph:

--As described above, with the manufacturing method of a semiconductor device in accordance with the present embodiment, the damaged layer (defective areas), such as a machining-affected layer and fine cracks, on the rear face of a semiconductor wafer resulting from the rear-face polishing process can be removed by the chemical etching; thus, it becomes possible to eliminate an unwanted stress exerted on the polished face and deflection in the semiconductor wafer, which have been conventional problems. Moreover, these effects are particularly advantageous in the manufacturing process of thin-film semiconductor wafers which have difficulties in transporting and handling.--

Please replace the paragraph beginning on page 50, line 25 with the following rewritten paragraph:

-- The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: semi-full dicing the semiconductor wafer from the front face (element formation face); forming a protective layer having a chemical etching resistant property on the front face of the semiconductor wafer; removing damaged areas (defective areas), such as a machining-affected layer and fine cracks, on a chip cut face resulting from the semi-full dicing process, by using chemical etching while the front face of the semiconductor wafer is being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing

state by the chemical etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.--

Please replace the paragraph beginning on page 52, line 4 with the following rewritten paragraph:

--Moreover, since the semiconductor wafer can be dealt on the basis of each piece as well as on the basis of one lot, it is superior in the working efficiency at the time of mass production, and particularly advantageous in the manufacturing process of thin-film semiconductor wafers which have difficulties in transporting and handling.--

Please replace the paragraph beginning on page 52, line 18 with the following rewritten paragraph:

-- The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: forming a protective layer having dicing resistant and chemical etching resistant properties on the front face (element formation face) of the semiconductor wafer; semi-full dicing the semiconductor wafer from the rear face of the semiconductor wafer; removing damaged areas (defective areas), such as a machining-affected layer and fine cracks, on a chip cut face resulting from the semi-full dicing process, by using chemical etching while the front face (element formation face) of the semiconductor wafer is being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing state by the chemical

etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.--

Please replace the paragraph beginning on page 53, line 19 with the following rewritten paragraph:

-- The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: after polishing the semiconductor wafer prior to dicing, semi-full dicing the semiconductor wafer from the front face (element formation face) or the rear face of the semiconductor wafer; forming a protective layer having a chemical etching resistant property on the front face of the semiconductor wafer; removing damaged areas (defective areas), such as a machining-affected layer and fine cracks, on the rear face of the semiconductor wafer resulting from the rear-face polishing process, as well as damaged areas (defective areas) on a chip cut face resulting from the semi-full dicing process, by using chemical etching while the front face of the semiconductor wafer being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing state by the chemical etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.--

Please replace the paragraph beginning on page 56, line 11 with the following rewritten paragraph:

-- In other words, in the chemical etching process, first, the semiconductor wafer is etched from the rear face thereof in the thickness direction of the semiconductor chip. At this time, the dicing residual portion is simultaneously etched from the rear face so that when the etching has reached the thickness of the dicing residual portion (dicing residual amount) left in the semi-full dicing process, the semiconductor wafer is divided into individual semiconductor chips. After the semiconductor chips have been separated, the etchant is allowed to enter a groove between the adjacent semiconductor chips formed in the semi-full dicing process, with the result that the semiconductor chip is etched also in the width direction from its cut face; thus, it is possible to remove damaged areas resulting from the semi-full dicing process.--

Please replace the paragraph beginning on page 60, line 13 with the following rewritten paragraph:

-- Furthermore, the manufacturing method of the semiconductor device in accordance with the present invention may include the rear-face polishing process for polishing the rear face that is the face opposite to the element formation face of the semiconductor wafer, prior to the semi-full dicing process, and may remove the damaged areas on the rear face of the semiconductor wafer resulting from the rear-face polishing process during the chemical etching process.--

Please replace the paragraph beginning on page 60, line 22 with the following rewritten paragraph:

-- The above-mentioned method makes it possible to remove damaged areas such as a machining-affected layer and fine cracks on the rear face of the semiconductor wafer resulting from the rear-face polishing process and damaged areas on a chip cut face resulting from the semi-full dicing process thereafter through the chemical etching process, while protecting the element formation face. Simultaneously with this process, the rear-face polishing process of the semiconductor wafer is carried out, and the dividing process into individual semiconductor chips from a semi-full dicing state is also carried out by removing the dicing residual portion.--

Please replace the paragraph beginning on page 62, line 11 with the following rewritten paragraph:

-- Consequently, the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production. This superior working efficiency at the time of mass production becomes particularly effective in the manufacturing process of thin-film wafers that have difficulties in transportation and handling.--

IN THE CLAIMS

Please replace claims 1-11 and 13-19 with the following rewritten claims:

1. (Amended) A manufacturing method for a semiconductor device comprising the steps of: